REMARKS

AMENDMENTS TO THE DETAILED DESCRIPTION OF THE INVENTION

Applicants respectfully submit that the amendments made to the Detailed Description of the Invention does not add any new matter since the amendment was performed to correct typographical errors.

AMENDMENTS TO THE DRAWINGS

Objection(s) to the drawings have been addressed. No new matter has been added.

OBJECTIONS TO THE CLAIMS

The Examiner objected to Claims 4 and 11 by requesting that the word MIPS be defined within the scope of the claims. Applicants respectfully submit that the meaning "MIPS" as described in the specification is well-known to one or ordinary skill in the art. The Examiner has requested that the Applicants consider amending Claims 4 and 11 by substituting the word MIPS with "Million Instructions Per Second {sic} (MIPS)", when it is well-known that MIPS stands for a RISC microprocessor architecture developed by MIPS Computer Systems, Inc. (aka MIPS Technologies). Applicants do not agree with Examiner's characterization and advice to amend; and as a consequence, Applicants have not amended Claims 4 and 11. It is unclear why the Examiner has objected to Claim 19. Both Claims 18 and 19 recite a "translation lookaside buffer" and the Applicants feel that there is no reason to amend these claims to include the acronym "TLB". The acronym "TLB" is clearly defined in the specification. As a consequence,

Applicants do not see reason to amend Claim 19, as the Examiner has advised. As a consequence, Applicants have not amended Claim 19.

35 USC § 102 REJECTIONS

CLAIMS 1-2, 6, 12-13, and 15-19

The Examiner has rejected Claims 1-2, 6, 12-13, and 15-19 under 35 U.S.C. 102(b) as being anticipated by Hinton et al. (US 5,500,948), hereinafter "Hinton".

As per independent Claims 1, 12, 16, and 18, the Examiner attempts to teach what is recited in these claims by referring to various excerpts of Hinton (Column 3, lines 23-25; Figure 1; Columns 5-6, lines 62-67 and 1-5; Columns 1-2, lines 64-67 and 1-29; Column 6, lines 37-63; Figure 3). However, the argument posed by the Examiner in Section 11 of the Office Action appears to make an attempt at addressing only Claim 1 of the instant Application.

With respect to Claim 1, the Examiner refers to Column 3, lines 23-25, and Figure 1, in an attempt to teach a translation lookaside buffer as recited in Claim 1. However, as stated in the Brief Description of the Drawings of Hinton, Figure 1 is "a block diagram of a microprocessor in which the present invention is embodied". Furthermore, there is no mention or disclosure of a translation lookaside buffer in Figure 1. The Examiner refers to Columns 5-6, lines 62-67 and 1-5, in an attempt to teach what is recited in Claim 1. However, Claim 1 recites "a method of reducing the size of a translation lookaside buffer comprising utilizing a bit obtained from a virtual page number of a virtual address for the purposes of writing and reading even and odd page frame numbers into a single page frame number field of said translation lookaside buffer".

Nowhere does Hinton disclose all the elements and features as recited in Claim 1. For example, Applicants have not found any mention of "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as recited in Claim 1. Furthermore, Hinton is different from the claimed invention of the instant Application. Hinton describes a translation lookaside buffer (TLB) *and* a translation write buffer (TWB) for implementing a data processing system (Column 7, lines 54-60) (emphasis denoted in italics). Therefore, Applicants respectfully submit that Claim 1 contains patentable subject matter that should be allowed. Since Claims 2-11 depend on an allowable Claim 1, these claims should be allowed as well. Therefore, for at least the foregoing reasons, Applicants respectfully request allowance of Claims 1-11.

As per Claim 2, Applicants respectfully submit that Hinton does not teach utilizing a bit that corresponds to a least significant bit of a virtual page number, as recited in Claim 2. In response to the Examiner's comment in section 12 of the Office Action (that references Column 6, lines 37-63; Figure 3) that "a logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page" and explains that "bit 12 selects which of the two entries in the TWB (62) are to be used for this address", the Applicants respectfully submit that "bit 12" is *not* (emphasis added in italics) a least significant bit as recited in Claim 2. As a consequence, for at least this reason alone, Applicants request allowance of Claim 2.

As per Claim 12, the Applicants fail to see how Hinton teaches what is recited in Claim 12. For example, nowhere does Hinton teach "a translation lookaside buffer comprising using a bit obtained from a virtual page number to consolidate even and odd page frame numbers into a

single page frame number field of said translation lookaside buffer", as recited in Claim 12. Nowhere does Hinton disclose or mention using "a bit obtained from a virtual page number" or "a single page frame number field of a translation lookaside buffer (TLB)". Furthermore, Hinton is different since Hinton discloses a data processing system comprising a translation lookaside buffer (TLB) and an improvement comprising "a logical address bus connected to said TLB and to said TWB, said logical address bus presenting an instruction pointer to the said TLB and to said TWB, said instruction pointer comprised of logical address bits including upper order bits, lower order bits, and a single bit having a first value or a second value, said single bit providing for translation of even-number pages for which said single bit has said first value and for odd-number pages for which said single bit has said second value" [Column 9, lines 26-30; Column 10, lines 6-16]. Therefore, Hinton's invention uses two buffers (i.e., a TLB and a TWB) compared to Applicants' claimed invention which uses a single buffer (i.e., a TLB). Therefore, for each of the foregoing reasons, the Applicants respectfully submit that Claim 12 contains patentable subject matter. Since Claims 13-15 are dependent on independent Claim 12, Applicants respectfully submit that these claims are allowable as well.

As per Claim 13, Applicants respectfully submit that Hinton does not teach utilizing a bit that corresponds to a least significant bit of a virtual page number, as recited in Claim 12. In response to the Examiner's comment in section 12 of the Office Action (that references Column 6, lines 37-63; Figure 3) that "a logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page" and explains that "bit 12 selects which of the two entries in the TWB (62) are to be used for this address", the Applicants respectfully submit that

"bit 12" is *not* (emphasis added in italics) a least significant bit as recited in Claim 13. As a consequence, for at least this reason alone, Applicants request allowance of Claim 13.

While the Applicants are unsure whether the Examiner has provided reasons for rejecting Claims 12, 16, and 18, the Applicants respectfully submit that nowhere in Hinton is there any teaching or disclosure of all the elements and/or features recited in these Claims. As per Claim 16, the Applicants fail to see how Hinton teaches what is recited in Claim 16. For example, nowhere does Hinton teach "a single page frame number field for storing odd/even page frame numbers", as recited in Claim 16. As a consequence, Applicants request the Examiner to withdraw her rejection to Claim 16. As per Claim 18, the Applicants fail to see how Hinton teaches what is recited in Claim 18. For example, nowhere does Hinton teach a "translation lookaside buffer using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field of said translation lookaside buffer", as recited in Claim 18. As a consequence, Applicants request the Examiner to withdraw her rejection to Claim 18.

35 USC § 103 REJECTIONS

CLAIMS 3, 5, 10, 14 and 20

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Thirdly, the prior art reference (or references when combined) must teach or suggest all the claim limitations

(emphasis denoted in italics). The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure (per § 2142 of the MANUAL OF PATENT EXAMINING PROCEDURE, 8th ed., Rev. 3 (August, 2005) [MPEP], Ch. 2100, p.134.).

For Claims 3, 5, 10, 14, and 20, the Examiner has admitted that Hinton does not expressly disclose "wherein said reading and writing is performed by way of using an existing translation lookaside buffer (TLB) control processor instruction set" and "wherein said translation lookaside buffer of reduced size is compatible with one or more legacy systems utilizing any existing TLB instructions, software, or commands". The Examiner has taken official notice that it "would have been obvious to one of ordinary skill in the art at the time the invention was made to use an existing translation lookaside buffer control instruction set and make the translation lookaside buffer as taught by Hinton compatible with existing TLB instructions, software, or commands as one of ordinary skill in the art would have been motivated to select from off the shelf processors at least to reduce cost and take advantage of existing system components." Applicants traverse and/or challenge the Examiner's official notice, and request that if the Examiner maintains (or wishes to maintain) the rejections for Claims 3, 5, 10, 14, and 20, that the Examiner produces documentary evidence to support her assertion. Applicants fail to see how the Examiner has established a prima facie case of obviousness. For at least the foregoing reasons, the Applicants request the Examiner to withdraw the rejections to Claims 3, 5, 10, 14, and 20. Applicants request allowance of Claims 3, 5, 10, 14, and 20.

Furthermore, in the Office Action, the Examiner states that "Furthermore, A [sic] recitation directed to the manner in which a claim is intended to be used does not distinguish the claim from the prior art if prior art has the capability to do so (See MPEP 2114 and Ex Parte Masham, 2 USPQ2d 1647 (1987)". The Applicants respectfully submit that MPEP 2114 may be applied to *apparatus claims* and not method claims (emphasis denoted in italics). The Applicants direct the Examiner to MPEP 2114, which is explicitly directed to apparatus and article claims. As recited from MPEP 2114: "A claim containing a "recitation with respect to the manner in which a claimed *apparatus* is intended to be employed does not differentiate the claimed *apparatus* from a prior art *apparatus*" if the prior art *apparatus* teaches all the structural limitations of the claim." (emphasis denoted in italics). As a consequence, the argument posed by the Examiner is not applicable and as a consequence, fails to justify the rejection to Claims 3, 5, 10, and 14. Hence, the Applicants request the Examiner to withdraw the rejections to these claims.

Turning to Claims 4 and 11, the Examiner has admitted that "Hinton does not disclose expressly that said TLB control processor instruction set comprises a MIPS control processor instruction set." Furthermore, the Examiner takes official notice by stating that: "It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an instruction set which comprises a MIPS (Millions Instructions Per Second) {sic} processor instruction set which is a well-known processor type. One of ordinary skill in the art would have been motivated to select from off the shelf processors at least to reduce cost and take advantage of existing system component designs." The Applicants respectfully submit that the Examiner's characterization of what is recited in Claims 4 and 11 is incorrect. Applicants submit that MIPS refers to a RISC microprocessor architecture developed by MIPS Technologies (aka MIPS

Computer Systems Inc.). Furthermore, Applicants traverse and/or challenge the Examiner's official notice, and request that if the Examiner maintains (or wishes to maintain) the rejections for Claims 4 and 11, that the Examiner produces documentary evidence to support her assertion. Applicants fail to see how the Examiner has established a prima facie case of obviousness. For at least each of the foregoing reasons, the Applicants request the Examiner to withdraw the rejections to Claims 4 and 11. Applicants request allowance of Claims 4 and 11.

The Examiner has rejected Claims 8-9 under 35 USC 103(a) as being unpatentable over Hinton in view of in view of Riedlinger et al. (US 6,446,187), hereinafter Riedlinger. The Examiner references Column 4, lines 14-23 of Riedlinger. However, nowhere does Riedlinger disclose a "page mask size ranging from 4 kilobytes to 16 megabytes" as recited in Claim 8. Applicants disagree with the Examiner that the "Applicant (sic) has not disclosed that [having a virtual address utilize a page mask ranging from 4 kilobytes to 16 megabytes or a page mask of 4 kilobytes] provides an advantage, is used for a particular purpose, or solves a stated problem." The Applicants respectfully submit that the page mask size as used in the various aspects of Applicants' claimed invention provides a preferred embodiment (i.e., a preferred range) in which the invention may be realized. As a consequence, Applicants request that the Examiner withdraw her rejection of Claim 8. Again, Claim 9 recites the method of Claim 8 wherein said page mask size comprises 4 kilobytes. Claim 9 provides another embodiment in which the various aspects of the invention may be practiced wherein the page mask size is 4 kilobytes. For at least the foregoing reasons alone, the Applicants request allowance of Claims 8-9.

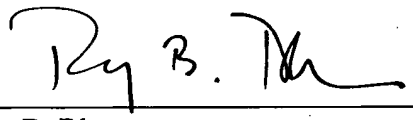
CONCLUSION

Based on at least the foregoing, the Applicants believe that Claims 1-20 are in condition for allowance. A Notice of Allowance is courteously solicited. Should anything remain in order to place the present application in condition for allowance, or should the Examiner disagree or have any question regarding this submission, the Examiner is kindly invited to contact the undersigned at (312) 775-8246.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Dated: July 25, 2006

Respectfully submitted,



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